UNITED STATES PATENT AND TRADEMARK OFFICE

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/725,663	DANILAK ET AL.
	Examiner	Art Unit	
	Chun-Kuan Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>06 October 2008</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-21</u> is/are pending in the application.

    4a) Of the above claim(s) <u>2-5,9-11 and 14-20</u> is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1,6-8,12,13 and 21</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>01 December 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date <u>09/26/2008</u>.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

CONTINUED EXAMINATION UNDER 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/06/2008 has been entered.

RESPONSE TO ARGUMENTS

2.   Applicant's arguments filed 10/06/2008 have been fully considered but they are not persuasive. Currently, claims 2-5 and 9-11 and 14-20 are withdrawn and claims 1, 6-8, 12-13 and 21 are pending for examination.

3.   In response to applicant's arguments (on page 10, last paragraph to page 13 1st paragraph and page 14, 2nd paragraph to page 15, 1st paragraph) with regard to the independent claim 1 rejected under 35 U.S.C. 103(a) that the combination of references does not teach/suggest the claimed feature that "the bypass register is memory mapped and implements aggregation of transaction information from a host CPU by using a memory mapped data transfer," because Chisholm does not teach/suggest memory

mapped data transfers, DMA transfers via memory mapped registers, or the like; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because Chisholm teaches a bypass register (Fig. 3, ref. 311), wherein the bypass register is memory mapped and implements aggregation (e.g. aggregation via transfer to accumulate) of transaction information (e.g. command block with transaction information for data transferring) from a host CPU (Fig. 3, ref. 103) by using a memory mapped data transfer (e.g. memory mapped data transfer corresponding to the transferring of the command blocks via memory mapping by command block address to the host memory) (col. 5, l. 1 to col. 6, l. 8), wherein the register (Fig. 3, ref. 311) is memory mapped as the register comprises the command block address received from the host CPU for transferring of the command/data blocks (Fig. 3, ref. 301) (e.g. transaction information) (col. 5, ll. 25-34), wherein the command block address is mapped to where the corresponding command/data block is located in the host memory (Fig. 3, ref. 107).

Additionally, Chisholm does teach the above memory mapped data transferring to be associated with DMA transfer as the DMA state machines (Fig. 3, ref. 322, 324) are utilized (col. 1, l. 52 to col. 2, l. 8 and col. 5, l. 1 to col. 6, l. 8).

As the applicant is also applying the above arguments presented for the independent claim 1 toward the independent claim 8, the examiner will also apply the above response toward the independent claim 8.

4.   In response to applicant's arguments (on page 13, 2nd paragraph to page 14, 1st

paragraph) with regard to the independent claim 1 rejected under 35 U.S.C. 103(a) that

the combination of references does not teach/suggest the claimed feature that the disk

I/O controller causing the startup of the disk drive upon receiving the command,

enabling the disk controller to hide the start up latency of the disk drive, and processing

this transaction information from a memory mapped bypass register; applicant's

arguments have fully been considered, but are not found to be persuasive.

       Please note one cannot show nonobviousness by attacking references

individually where the rejections are based on combinations of references. See *In re*

Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091,

231 USPQ 375 (Fed. Cir. 1986). The examiner relied on the prior art as following for the

teaching of the above claimed features:

       Chisholm teaches the disk I/O controller processing disk transaction information

from a memory mapped bypass register (Fig. 3 and col. 5, l. 1 to col. 6, l. 8).

       Wood teaches the disk I/O controller (Fig. 3, ref. 314) causing the startup of the

disk drive (Fig. 3, ref. 318) upon receiving the command (e.g. start command) (col. 3, ll.

10-27 and col. 6, ll. 1-65).

       Davis teaches enabling the disk controller to hide the start up latency of the disk

drive (col. 1, l. 61 to col. 2, l. 3), in combination with Chisholm's disk controller and

Wood's start up command; the resulting combination of the references teach that the

start up latency for the disk drive is hidden via the number of data queue as delay

associated with the requesting and obtaining access (e.g. start up command) to a bus

coupled to a corresponding peripheral is hidden.

As the applicant is also applying the above arguments presented for the

independent claim 1 toward the independent claim 8, the examiner will also apply the

above response toward the independent claim 8.

5.   In response to applicant's arguments (on page 14, 2nd paragraph) with regard to

the independent claim 1 rejected under 35 U.S.C. 103(a) that <u>Chisholm</u> does not

teach/suggest a bus master controller coupled to the disk I/O engine, a bypass register

coupled to the bus master controller, an arbiter coupled to the bus master controller and

the disk I/O engine; applicant's arguments have fully been considered, but are not found

to be persuasive.

Please note one cannot show nonobviousness by attacking references

individually where the rejections are based on combinations of references. See *In re*

Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091,

231 USPQ 375 (Fed. Cir. 1986). The examiner relied on the prior art as following for the

teaching of the above claimed features:

<u>Chisholm</u> teaches a disk controller (Fig. 3, ref. 201, 203, 209, 213) comprising a

bypass register (Fig. 3, ref. 203, 311) and a disk I/O engine (Fig. 3, ref. 209, 213) (col.

5, l. 1 to col. 6, l. 8).

<u>Winkler</u> teaches a system and a method comprising:

a bus master controller coupled to a disk I/O engine (e.g. hard disk controller) [0013], in combination with <u>Chisholm</u>'s teachings, the bypass register which is coupled to the disk I/O engine is coupled to the bus master controller; and

an arbiter coupled to the bus master controller and the disk I/O engine (e.g. hard disk controller), to coordinate data transfers within the disk controller [0013].

As the applicant is also applying the above arguments presented for the independent claim 1 toward the independent claim 8, the examiner will also apply the above response toward the independent claim 8.

6.   In response to applicant's arguments (on page 15, 3rd paragraph) with regard to the dependent claims 6 and 12 rejected under 35 U.S.C. 103(a) that the combination of references does not teach/suggest the claim limitations recited in the claims; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, as <u>Chisholm</u> and <u>Winkler</u> teach the bridge component wherein the disk controller further comprising a CPB pointer buffer (<u>Chisholm</u>, command address queue 309 of Fig. 3) coupled to the disk I/O engine for dynamically appending a plurality of CPB pointers (e.g. addresses pointing to where the command block are stored) to extend to a number of disk transactions scheduled for execution by the disk I/O engine, the CPB pointer buffers (<u>Chisholm</u>, Fig. 3, ref. 309) directly connected to the disk I/O engine (<u>Chisholm</u>, Fig. 3, ref. 209, 213) for control independent of the arbiter (<u>Chisholm</u>, col. 5, l. 1 to col. 6, l. 8 and <u>Winkler</u>, [0013]).

7.   In response to applicant's arguments (on page 15, last paragraph to page 16, 1st

paragraph) with regard to the new independent claim 21 rejected under 35 U.S.C.

103(a) that the combination of references does not teach the claimed feature a chain

memory coupled to the disk I/O engine for buffering a plurality of CPBs to extend a

number of disk transactions scheduled for execution by the disk I/O engine; applicant's

arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because <u>Chisholm</u> teaches a chain

memory (e.g. section of the memory 203 storing the command blocks 304 of Fig. 3,

wherein the memory section is the chain memory storing the chain of command blocks

as the addresses (Fig. 3, ref. 309) pointing to these command blocks are in a chain)

coupled to the disk I/O engine (Fig. 3, ref. 209, 213) for buffering a plurality of CPBs

(Fig. 3, ref. 304) to extend a number of disk transactions scheduled for execution by the

disk I/O engine (col. 5, l. 1 to col. 6, l. 8).

Additionally, it is not fully clear to the examiner as to where in the Specification or

the Drawings disclose that the chain memory and its functionality is separate and

distinct from the operation of the bypass register.

I. <u>ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT</u>

8.   As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information

Disclosure Statement dated September 26, 2008 is acknowledged by the examiner and

the cited references have been considered in the examination of the claims now

pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

II. OBJECTIONS TO THE CLAIMS

Claims 1, 7-8, 13 and 21 are objected to because of the following informalities:

in claim 1, line 9, "transaction information" should be replace with -disk transaction information-.

in claim 7, line 3, "to extend to a number of disk transactions" should be replace with -to extend a number of disk transactions-.

in claim 8, line 11, "transaction information" should be replace with -disk transaction information-.

in claim 13, line 3, "to extend to a number of disk transactions" should be replace with -to extend a number of disk transactions-.

in claim 21, line 9, "transaction information" should be replace with -disk transaction information-.

in claim 21, line 14, "to extend to a number of disk transactions" should be replace with -to extend a number of disk transactions-.

Appropriate correction is required.

III. REJECTIONS BASED ON 35 U.S.C. 112

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

9.   Claims 1 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being

incomplete for omitting essential elements, such omission amounting to a gap between

the elements. See MPEP § 2172.01. The omitted elements are: a chain memory for

buffering the CPBs to extend a number of disk transactions scheduled for execution by

the disk I/O engine.

As per claims 1 and 8, in view of the Drawings in Figures 17-18, it seems it would

be essential for the inclusion of the chain memory in the disk controller for proper

implementation of the claimed invention.

IV. <u>REJECTIONS BASED ON PRIOR ART</u>

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

10.   Claims 1, 6-8, 12-13 and 21 are rejected under 35 U.S.C. 103(a) as being

unpatentable over <u>Chisholm et al.</u> (US Patent 5,968,143) in view of <u>Wood et al.</u> (US

Patent 6,915,363), <u>Davis et al.</u> (US Patent 6,298,407) and <u>Winkler et al.</u> (US Pub:.

2004/0024948).

11.   As per claims 1, 8 and 21, <u>Chisholm</u> teaches a bridge component for

implementing efficient disk I/O for a computer system, comprising:

a bus interface (Fig. 3, ref. 109, 111) for interfacing with a processor (Fig. 1, ref.

103) and a system memory (Fig. 3, ref. 301) of the computer system;

a disk controller (Fig. 3, ref. 201, 203, 209, 213, 311) for executing disk

transactions for the computer system, the disk controller further comprising:

a disk I/O engine (Fig. 3, ref. 209, 213) coupled to the bus interface;

a bypass register (Fig. 3, ref. 203, 311) coupled to the disk I/O engine, wherein

the bypass register is memory mapped and implements aggregation (e.g. aggregation

via transfer to accumulate) of disk transaction information (e.g. command block with

transaction information for data transferring) from a host CPU (Fig. 3, ref. 103) by using

a memory mapped data transfer (e.g. memory mapped data transfer corresponding to

the transferring of the command blocks via memory mapping by command block

address to the host memory) (col. 5, l. 1 to col. 6, l. 8), wherein the register (Fig. 3, ref.

311) is memory mapped as the register comprises the command block address

received from the host CPU for transferring of the command/data blocks (Fig. 3, ref.

301) (e.g. transaction information) (col. 5, ll. 25-34), wherein the command block

address is mapped to where the corresponding command/data block is located in the

host memory (Fig. 3, ref. 107);

a chain memory (e.g. section of the memory 203 storing the command blocks

304 of Fig. 3, wherein the memory section is the chain memory storing the chain of

command blocks as the addresses (Fig. 3, ref. 309) pointing to these command blocks

are in a chain) coupled to the disk I/O engine (Fig. 3, ref. 209, 213) for buffering a

plurality of CPBs (Fig. 3, ref. 304) to extend a number of disk transactions scheduled for

execution by the disk I/O engine (col. 5, l. 1 to col. 6, l. 8); and

a device interface (Fig. 2, ref. 217) coupled to the disk I/O engine (Fig. 3, ref.

209, 213) for interfacing the disk I/O engine with a disk drive (e.g. SCSI RAID disk

drives) (Fig. 1, ref. 114; Fig. 2, ref. 115 and col. 4, ll. 26-36), the disk I/O engine further

configured to execute a disk transaction by processing the disk transaction information

(Fig. 3, ref. 304) from the memory mapped bypass register (Fig. 3, ref. 203, 311)

coupled to the disk I/O engine (col. 5, l. 1 to col. 6, l. 8), as the command/data blocks

are transferred to the memory mapped bypass register for implementing disk

transaction and bypass the writing of a set of 8 bit registers in the disk controller as

implemented in ATA disk drives.

Chisholm does not teach the bridge component comprising a bus master

controller ...; an arbiter coupled to the bus master controller ...; and wherein the disk I/O

engine is configured to cause a start up of the disk drive upon receiving a disk start up

command from the processor, the start up command configured to hide a start latency

of the disk drive.

Wood teaches a system and a method comprising

a host computer (Fig. 3, ref. 302);

an array of disk drives (Fig. 3, ref. 318) comprising a redundant array of

Inexpensive discs (RAID) (col. 1, ll. 47-51);

transferring a start command to the array of disk drives via a subsystem

controller (Fig. 3, ref. 314) to cause the array of disk drives to start up, as the timing for

transferring the start command to each disk drive is controlled and regulated (col. 3, ll.

10-27 and col. 6, ll. 1-65).

It would have been obvious to one of ordinary skill in this art, at the time of

invention was made to include Wood's start command into Chisholm's bridge

component for the benefit of enabling proper start up of the array of disk drives utilizing

out-of-band signaling without exceeding the capability of the power supply (Wood, col.

1, ll. 52-60 and col. 3, ll. 1-9) to obtain the invention as specified in claims 1 and 8. The

resulting combination of the references further teaches the bridge component

comprising wherein the subsystem controller (e.g. disk I/O engine) is configured to

cause the disk drive to start up as the start command (e.g. disk start up command) is

received from the host computer (e.g. processor).

Chisholm and Wood do not teach the bridge component comprising a bus master

controller ...; an arbiter coupled to the bus master controller ...; and wherein the start up

is configured to hide a start latency of the disk drive.

Davis teaches a bridge component comprising a number of data queues

implemented to hide the delay associated with the requesting and obtaining access to a

bus coupled to a corresponding peripheral as data can be transferred without delay (col.

1, l. 61 to col. 2, l. 3).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Davis's data queues into Chisholm and Wood's bridge component for the benefit of synchronizing the transferring of data between the initiator and the target (Davis, col. 2, ll. 10-13) to obtain the invention as specified in claims 1 and 8. The resulting combination of the references further teaches the bridge component comprising wherein the subsystem controller (e.g. disk I/O engine) is configured to cause the disk drive to start up as the start command (e.g. disk start up command) is received from the host computer (e.g. processor), wherein the start command would be configured to hide the delay associated with the disk drive's start latency, as data to be transferred can be send following the transferring of the start command without delay.

Chisholm, Wood and Davis do not expressly teach the bridge component comprising a bus master controller ...; and an arbiter coupled to the bus master controller ... .

Winkler teaches a system and a method comprising:

a bus master controller coupled to a disk I/O engine (e.g. hard disk controller) [0013], in combination with the above teachings, the bypass register which is coupled to the disk I/O engine is coupled to the bus master controller; and

an arbiter coupled to the bus master controller and the disk I/O engine (e.g. hard disk controller), to coordinate data transfers within the disk controller [0013], wherein the

inclusion of the arbitration function into the disk controller would enable proper coordination of the data transferring for disk drive system such as RAID.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Winkler's bus master controller and arbitration into Chisholm, Wood and Davis's disk controller for the benefit of increasing the operation speed, as well as improving reliability and the efficiency in the transferring of data (Winkler, [0017]) to obtain the invention as specified in claims 1 and 8.

12.   As per claims 6 and 12, Chisholm, Wood, Davis and Winkler teach all the limitations of claims 1 and 8 as discussed above, where Chisholm and Winkler further teach the bridge component wherein the disk controller further comprising a CPB pointer buffer (Chisholm, command address queue 309 of Fig. 3) coupled to the disk I/O engine for dynamically appending a plurality of CPB pointers (e.g. addresses pointing to where the command block are stored) to extend to a number of disk transactions scheduled for execution by the disk I/O engine, the CPB pointer buffers (Chisholm, Fig. 3, ref. 309) directly connected to the disk I/O engine (Chisholm, Fig. 3, ref. 209, 213) for control independent of the arbiter (Chisholm, col. 5, l. 1 to col. 6, l. 8 and Winkler, [0013]).

13.   As per claims 7 and 13, Chisholm, Wood, Davis and Winkler teach all the limitations of claims 1 and 8 as discussed above, where Chisholm teaches the bridge component wherein the disk controller further comprising a chain memory (Chisholm,

section of the memory 203 storing the command blocks 304 of Fig. 3, wherein the

memory section is the chain memory storing the chain of command blocks as the

addresses (Fig. 3, ref. 309) pointing to these command blocks are in a chain) coupled to

the disk I/O engine for buffering a plurality of CPBs (Chisholm, Fig. 3, ref. 304) to extend

a number of disk transactions scheduled for execution by the disk I/O engine (Chisholm,

col. 5, l. 1 to col. 6, l. 8).

V. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1, 6-8, 12-13 and 21 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C.K.L./

October 28, 2008

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181